CONNOTECH Experts-conseils inc.
PPCMB/850 Product Family Documentation

PPCMB/850 Hardware User's Guide

(system engineering support document)

Document Number C001954

2003/09/29

Table of Contents

List of figures

List of Tables

Document Revision History

C-Number	Date	Explanation
C001249	2002/10/17	First Release
C001516	2003/02/03	Major document enhancements
C001607	2003/04/07	Inverted the RS422 signal polarity (figure 7 and table 4)
C001954	2003/09/29	Added section 5.6, jumper specification D1 <-> J1, D25, updated MPC850 document references
C001954		Current version

1. Introduction

The present document describes the PPCMB/850 digital electronics printed circuit board. It is intended both as a *hardware user's guide*, and to some extent as a *design planning guide* for system hardware designers. The Motorola MPC850 embedded processor documentation is an essential reading along with the present document. The MPC850 hardware documentation is in the references [1], [2], [3], [4], and [5].

The software aspects of the PPCMB/850 product is outside the scope of the present document. A goal of this document is to make the PPCMB/850 hardware useful with any embedded software development approach.

Nonetheless, the reader may refer to the CONNOTECH web site for the latest news and releases about software development tools, the ABCD Proto-Kernel™, and other software and utilities offered by CONNOTECH. Many of the software items originated from CONNOTECH are *free software* under the GNU-type licensing. Still, CONNOTECH recognizes the embedded system developers' needs for keeping their application software code proprietary and secret.

2. Overview

The core of the PPCMB/850 is the Motorola MPC850 embedded processor. As a manufacturing option, the PPCMB/850 may have a Motorola MPC823 or MPC823E processor instead, totally pin-compatible with the MPC850 (essentially, the MPC823 has an on-chip LCD and video controller that uses general-purpose parallel I/O pins available with the MPC850 as well). In this document, we make no further references to the MPC823 except if minor differences exist.

The PPCMB/850 is a complete processor implementation with its support electronics, memory subsystem, one serial port, and the required connectors for integration in an embedded system (see figure 1 on page 6). While the usual organization is a single board computer with *expansion board* connectors, the PPCMB/850 is best seen as a CPU piggyback module with *host application board* connectors. In terms of integration and time-to-market, it makes sense to design an embedded system board with just the exact set of peripherals and their specific front-end electronics and connector requirements, while using the off-the-shelf PPCMB/850 CPU module.

The mechanical arrangement and the connector locations for the PPCMB/850 are shown in figure 2 on page 7. Except for the connectors, the component height clearance is less than 0.1 inches on each side, with a printed circuit thickness of 0.062 inches. The parts that require the greater heat dissipation characteristics are on the top side of the PCB, namely the MPC850 processor and the SRAM memory ICs. The flash memory is on the bottom side of the PCB.

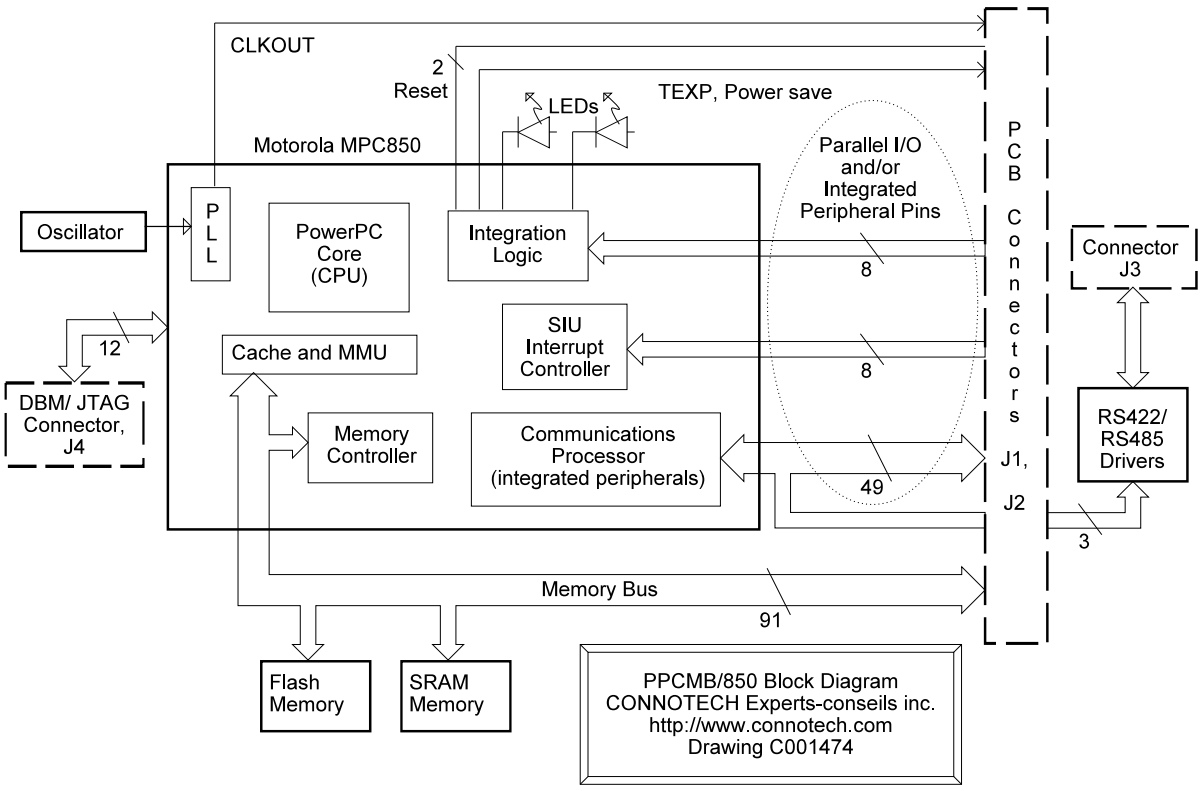

Figure 1. PPCMB/850 Block Diagram

3. Related Manufacturers' Documents

[1] Motorola, *MPC850 Family User's Manual - Integrated Communications Microprocessor*, document MPC850UM/D Rev. 1, 1/2001

[2] Motorola, *Errata to MPC850 Family User's Manual, Rev 1*, document MPC850UMAD/D Rev. 0.3, 6/2002

[3] Motorola, *MPC850 (Rev. A/B/C) Family Communications Controller Hardware Specifications*, document MPC850ABEC/D Rev. 1, 10/2002

[4] Motorola, *MPC850 Device Errata Reference*, Rev. 3, 2/2003

[5] Motorola, *MPC850 Family Device Errata Summary* Revision 2.1, 2/24/03

[6] AMD datasheet, *Am29LV160D, 16 Megabit (2 M x 8-Bit/1 M x 16-Bit), CMOS 3.0 Volt-only Boot Sector Flash Memory*, Publication# 22358 Rev: B Amendment/+3, Issue Date: November 10, 2000

[7] Sipex Corporation datasheet, *SP3490/SP3491 +3.3V Low Power Full Duplex RS-485 Transceivers with 10Mbps Data Rate*, document SP3490/3491DS/23

[8] Samtec, *2mm SQ Tail Socket SQT Series*, Factsheet F-202-1

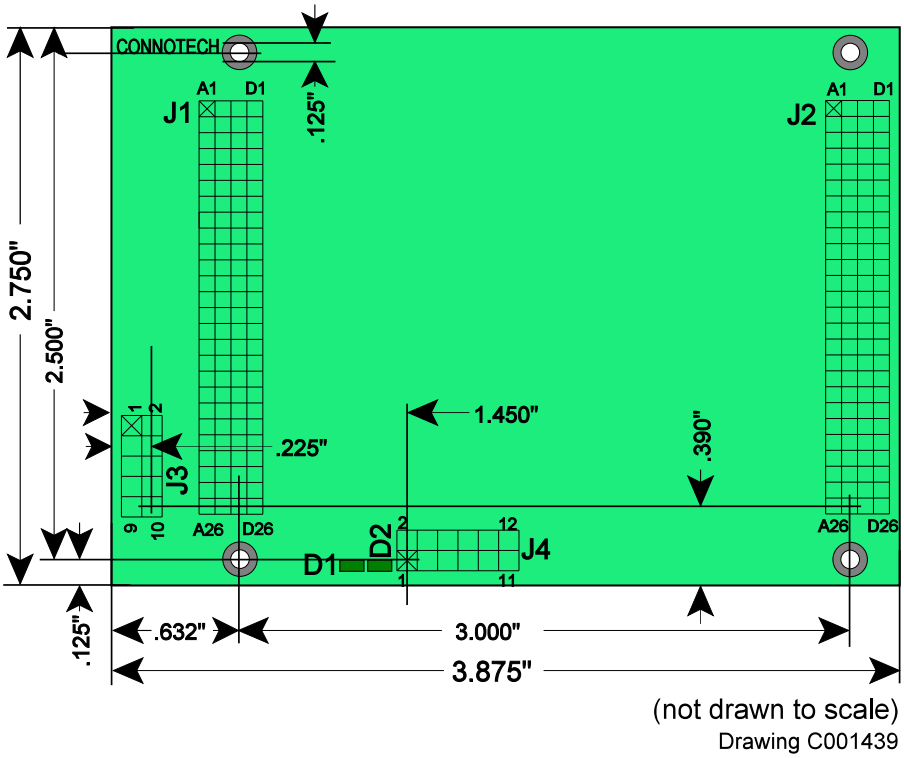

Figure 2. PPCMB/850 Mechanical Dimensions, Top side of PCB

4. Power Considerations

4.1 Power Supply

A regulated 3.3V power source must be externally supplied to the PPCMB/850. The MPC850 contains an internal analog SPLL (System Phase Lock Loop) circuit for clock frequency

multiplication with specific requirements for power noise filtering (on the VDDSYN pin). This filtering is implemented on the PPCMB/850 itself. The external power source should be a normal 3.3V power source adequate for digital electronics connected to the J1 and/or J2 pins as shown in figure 3 on page 8.

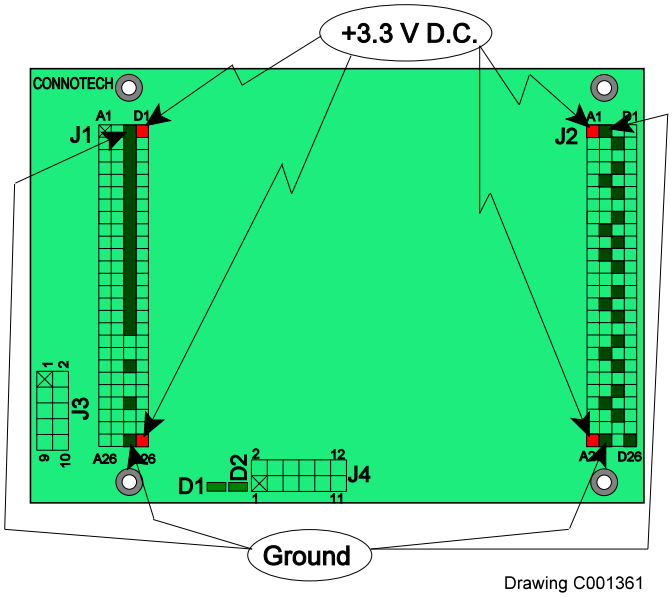

Figure 3. PPCMB/850 Power Supply Contacts

4.2 Power Management Support

The single 3.3V power is applied without distinction to the VDDH, VDDL, and KAPWR pins. This prevents the effective use of the MPC850 «deep sleep» and «power-down» modes (power consumption about 10 µA), and the time counting by the MPC850 real-time clock while the main power is turned off.

The power management modes of the MPC850 in which the SPLL remains active are available to the system hardware designer. For instance, a self-paced data monitoring system can enter the sleep mode (typical MPC850 consumption less than 10mW at 50MHz) between the monitoring process cycles.

The PPCMB/850 flash memory subsystem is readily available for permanent storage of system configuration. The CONNOTECH developed FlashCnL (Flash Configuration and Log) software hides the flash organization complexity for embedded applications. This use of a few flash sectors for storage of system configuration alleviates the need of battery backed-up memory in the system design.

5. Embedded Microprocessor Implementation

The figure 4 on page 9 shows the MPC850 support circuits implemented on the PPCMB/850.

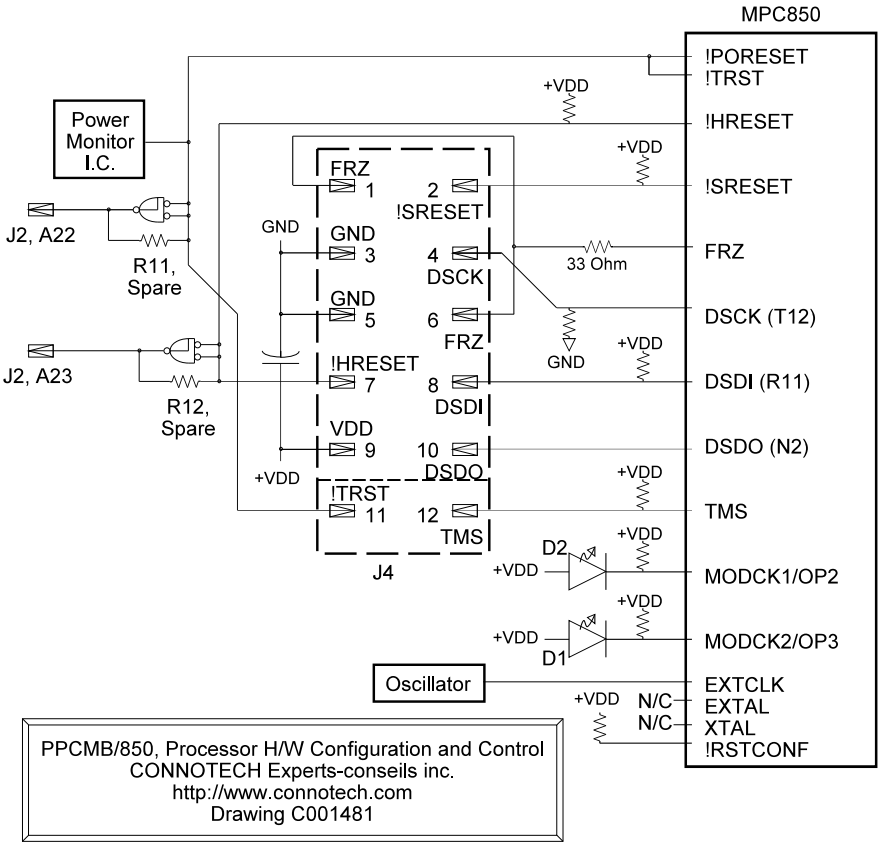

Figure 4. PPCMB/850 Processor H/W Configuration and Control

5.1 Reset Control

5.1.1 The Power-on Reset Signal (!PORESET)

The power level is monitored by a reset monitor circuit. The reset monitor circuit ensures that the !PORESET signal is held low for at least 250 ms when the power is applied to the board. This ensures a predictable and reliable power-up sequence.

Note: There is an unsafe voltage range below the MPC850 minimal input voltage (3.0 Volts up to 40 MHz, 3.135 Volts at higher frequencies) and above the reset monitor detection threshold (2.9 Volts typical). The power supply electronics should be designed to minimize the likelihood of steady operation within this unsafe voltage range.

5.1.2 The Hard Reset Signal (!HRESET)

The !HRESET hard reset signal is a bidirectional MPC850 signal that enables the software or the hardware to force a PPCMB/850 reset sequence nearly identical to a power-on reset. The MPC850 internally implements a 512 clock counter and related control logic to ensure a minimal duration of the !HRESET pulse and a clean reset sequence.

5.1.3 Reset Signals Availability on the Host Application Board Connectors

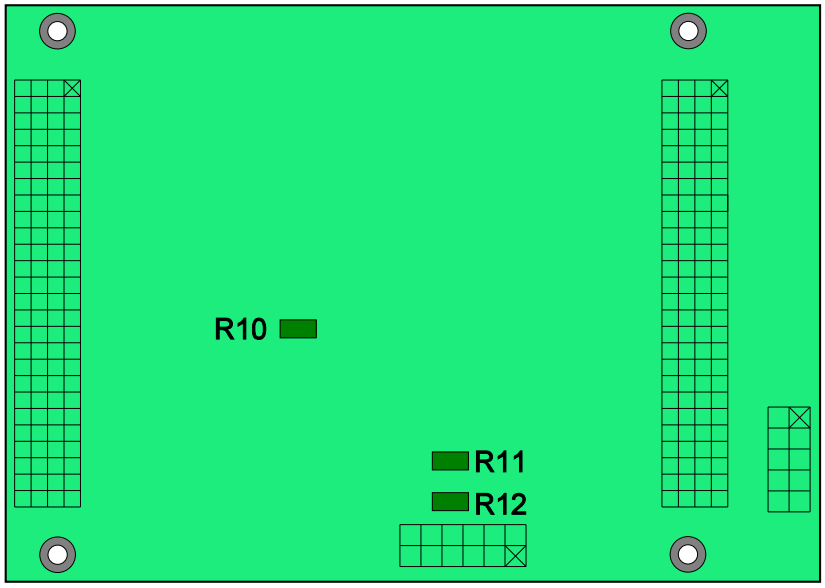

Figure 5. Component Locations on the Bottom Side of the PCB

The power-on reset and the hard reset signals are available on the J2 connector for use by the system application electronics. Since they are bidirectional signals, the lack of a protection mechanism would let the application electronics cause resets at will. As a protection mechanism against spurious resets originating from the application electronics, the PPCMB/850 buffers the !PORESET and !HRESET signals. The most likely use of these signals by the application electronics is the connection of !HRESET signal to the reset input of major digital components.

If the application electronics must be allowed to trigger a power-on reset cycle, a “0805” 0-Ohm resistor (shunt) can be installed on the resistor location R11 to bypass the !PORESET signal protection. Similarly, if the application electronics must be allowed to trigger a hard reset cycle, a “0805” 0-Ohm resistor (shunt) can be installed on the resistor location R12 to bypass the !HRESET signal protection. The figure 5 on page 10 shows the resistors locations on the PPCMB/850 PCB.

5.1.4 The Soft Reset Signal (!SRESET)

The !SRESET soft reset signal is routed to the BDM/JTAG connector J4. Since the !SRESET function is relevant only to software control of the processor through the BDM port, the system hardware designer should not be concerned with the !SRESET signal.

5.2 Processor Clock

The clock source is an external oscillator circuit. Its possible frequency range is from 3 to 10 MHz. The MPC850 clock configuration is such that the PPCMB/850 boots with a SPLL multiplication factor of 5. Accordingly, the possible default MPC850 operating frequency is between 15 and 50 MHz. The system clock configuration defined by the hardware at reset can be altered by the software.

The oscillator circuit frequencies currently available as manufacturing options are indicated in table 10 on page 27.

[[CONNOTECH developed a spreadsheet for clock configuration throughout the MPC850 functional blocks]]

5.3 MPC850 Configuration

The MPC850 hard reset configuration word is left to its default value, that is zero. In addition, the MODCK1 and MODCK2 signals are asserted (pulled up at +VDD level) at reset. Accordingly, the following MPC850 hardware configuration options apply at system reset time:

System clock configuration:

- The SPLL clock source input is the EXTCLK signal. This same clock source is applied to the time base and decrementer clock since the SCCR(TBS) field is zero. Also, this same clock source is applied to the PIT (Programmable Interval Timer) and the RTC (Real-Time Clock) since the SCCR(RTSEL) field is set to one.

- The SPLL multiplication factor is 5 since the PLPRCR(MF) field is 4.

- The SCCR(EBDF) field is zero, which implies that the external bus frequency is the same as the SPLL output.

- The time base and decrementer clock prescaler divisor is set to 4.

- The SCCR(RTDIV) field is one, which implies that the PIT and RTC clock prescaler divisor is set to 512.

Memory configuration

- The SIUMCR(EARB) field is zero, which implies that the MPC850 acts as a memory bus arbitration master.

- The core memory access operates in big endian mode during boot time (from reference [2]).

- The memory controller BR0(PS) field is zero and the BR0(V) field is one, which implies that the system boots from the 32 bits flash memory selected by the CS0 signal.

- The core CPU MSR(IP) field is set to 1, which implies that the first instruction fetched by the CPU is at address 0xFFF00100 (one megabyte below the top of flash memory, plus the 0x100 offset for the PowerPC reset exception vector).

  Note: The CONNOTECH developed FlashCnL (Flash Configuration and Log) software can take control of the flash memory sector that includes the 0xFFF00100 address. With this arrangement, the boot sequence jumps to a fixed address selected according to software design considerations, and the flash sector space is efficiently used for storage of system configuration data.

- The boot device does not support bursting (from reference [2]).

- The IMMR(ISB) field is zero, which implies that the MPC850 internal memory is located at address zero.

Debug pins configuration:

- The SIUMCR(DBGC) field is zero, which implies that parallel input signals IPB[0..7] are enabled and the LED control output signals OP[2..3] are enabled (both LEDs are turned on).

- The SIUMCR(DBPC) field is zero, which allows the PPCMB/850 J4 pins 4, 8, and 10 to

operate as a BDM port.

The MPC850 configuration defined by the hardware at reset can be altered by the software. In addition, the MPC850 is a highly configurable device. The configuration items not listed above are controlled by the software. Their default values at reset are fixed according to the MPC850 documentation.

The PPCMB/850 RS422/RS485 serial port configuration is documented in the next section.

5.4 Diagnostic LEDs

The two PPCMB/850 diagnostic LEDs are entirely software-controlled. The two output signals of the MPC850 PCMCIA interface are dedicated to the PPCMB/850 diagnostic LEDs. They are controlled through the PGCRB register. The bit position PGCRB(CBOE) controls the LED labeled D1, and the bit position PGCRB(CBRESET) controls the LED labeled D2. A zero at a bit position in the PGCRB register turns on the corresponding LED. The two relevant bit positions are shown in the table 1 on page 13, along with the various names affixed to the electrical link between the bits and the LEDs.

PGCRB Bit Weight	PGCRB Bit Name	PCMCIA Signal Name	MPC850 Signal Name	MPC850 Pin	PPCMB/850 LED Label
0x40	CBRESET	RESET_B	OP3/MODCK2	B6	D1
0x80	CBOE	POE_B	OP2/MODCK1	D6	D2

Table 1. PPCMB/850 Diagnostic LEDs Connectivity

5.5 Development Support with the BDM / JTAG Port

The J4 header connector on the PPCMB/850 is the BDM/JTAG connector for in-system debugging support. It uses a 2 x 6 contacts arrangement, of which the first 2 x 5 contacts use a Motorola recommended pinout for the BDM connection (see table 2 on page 14). There are two alternate BDM port pinouts in the Motorola documentation. The PPCMB/850 implements the simpler alternative where the coarser FRZ signal replaces the finer VFLS0 and VFLS1 signals for real-time program trace. Many third party tools vendor support this specifications.

The last two contacts on the J4 BDM/JTAG connector are provided for future support of JTAG tools. The pull-up resistor on the TMS signal ensures that the JTAG mode is not entered when the J4 pin 12 is left unconnected, but would allow a JTAG tool to take control of the processor upon reset. Before relying on the JTAG connection, a system hardware designer should check the JTAG support status with CONNOTECH.

Pin	Signal Name	Description
1	FRZ	Freeze status signal from the MPC850
2	!SRESET	Bidirectional Soft Reset signal
3	GND	Ground connection
4	DSCK	Development Serial Clock, clock for the MPC850 debug port interface.
5	GND	Ground connection
6	FRZ	Freeze status signal from the MPC850
7	!HRESET	Bidirectional Hard Reset signal
8	DSDI	Development Serial Data Input, data input to the MPC850 debug port interface.
9	VDD	+VDD (3.3 Volts) connection on the PPCMB/850
10	DSDO	Development Serial Data Output, output data from the MPC850 debug port interface
11	!TRST	Bidirectional Test Reset signal, connected to the MPC850 !TRST and !PORESET (not used for BDM connection)
12	TMS	Test mode select input t the MPC850 (not used for BDM connection)

Table 2. PPCMB/850 BDM/JTAG Connector J4 Pinout

5.6 Special Firmware Activation with Momentary Wire Jumper

The present specification is established to allow compatible firmware to be developed and factory-programmed into the PPCMB/850 flash memory through the BDM port. Thereafter, the BDM port becomes useless, so a PPCMB/850 user can avoid the cost and burden of a BDM interface and the associated software utilities. This can also be useful in the context of shop repair procedures, as a software error recovery procedure.

Here is the recommended special firmware activation procedure. Special firmware may be activated if a momentary wire connection is made between the PPCMB/850 PCB pin D15 on the J1 connector and the cathode side of the LED labeled D1 when the system is reset. From the processor perspective, this is a connection between the OP3 signal and the PB[27] signal, with an external pull-up. On the PCB, the momentary connection is depicted on figure 6 on page 15.

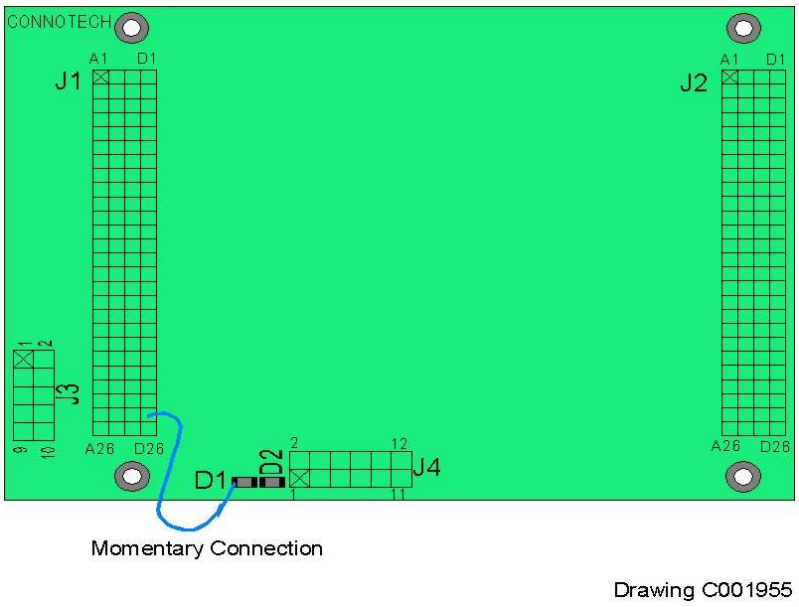

Figure 6. Momentary Wire Connection for Special Firmware Activation

Notes: 1) CONNOTECH Experts-conseils inc. provides some *embedded target loader firmware* as part of the ABCD Proto-Kernel™ distribution. This embedded target loader is compatible with the present specification.

2) Other firmware developers are invited to adopt the present specification in order to facilitate product family support. If the special firmware activation must be "password protected" in some ways, it is suggested to embed the password protection into the firmware protocol (instead of adopting another special firmware activation procedure).

3) A sample scenario for the use of special firmware activation is as follows: the PPCMB/850 flash memory contains an embedded target loader and an application software. The normal field-upgrade capability is made available to the system end-user as a special command sequence in the application software, that jumps into the embedded target loader that, in turn, loads the new application software (overwriting the existing one). In the exceptional case where the new application software is broken (either as a whole or just the special command sequence), the user is left with no way to load a new application software. The damaged unit proceeds through the shop repair procedure where the special firmware activation (with momentary wire jumper) forces the entry into the embedded target loader that, in turn, loads a (presumably defect-free) application software. In theory, although very unlikely in practice, the embedded target loader itself could be erased by a broken application software. In this case, a "manufacturer repair" procedure is needed, where the BDM interface is used to re-program the flash memory from scratch.

6. RS422/RS485 Communications Port

6.1 RS422/RS485 Serial Port Overview

See the figure 7 on page 17 for the RS422/RS485 serial port. The PPCMB/850 connector J3 is used for the RS422/RS485 serial port. The connector pinout is listed in table 3 on page 18. The J3 connector positions 1 to 6 are used for RS422/RS485 driver/receiver configuration. The J3 connector positions 7 to 10 are the differential transmit and receive signal pairs.

The RS422/RS485 interface IC avoids CMOS level signals that would leave the electronics subassembly comprising the PPCMB/850 and its host application PCB, according to recommended digital design practice.

The RS422/RS485 driver/receiver integrated circuit is a Sipex Corporation SP3491 part (the datasheet is reference [7]). The Maxim Integrated Products MAX3491 or MAX3491E parts are compatible. The Linear Technology LTC491 part is another functional equivalent, except that it is a 5 Volts only component. The datasheets and application notes from these manufacturers and the B&B Electronics web site (http://www.bb-elec.com/support.asp) provide useful sources of information about the RS422/RS485 networking technology.

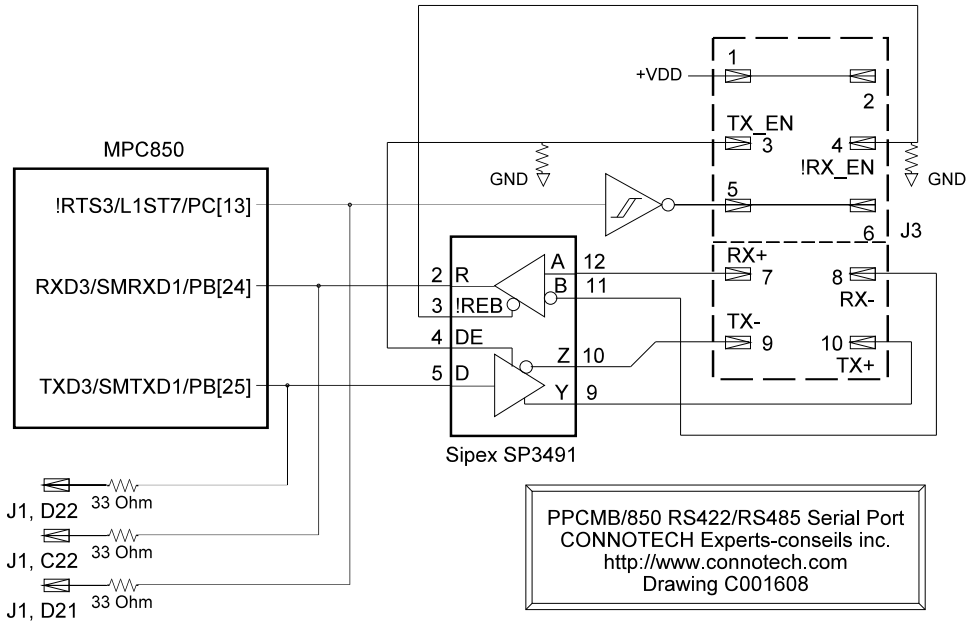

Figure 7. PPCMB/850 RS422/RS485 Serial Port

6.2 Network Design Issues

Thus, the PPCMB/850 RS422/RS485 serial port implements a minimal subset of diverse interconnect solutions that can potentially support a wide range of communication speeds, data and/or clock encoding options. Moreover, there are many compatible network interface topologies, cabling specs, and termination, EMC/EMI, ESD protection and isolation strategies. The required RS422/RS485 support electronics should be provided by the system component connected to J3. The underlying RS422/RS485 networking design issues were left out of the PPCMB/850 design. In line with this approach, no “signal ground” contact is provided on the J3 connector.

For high speed networking applications, the system hardware designer should pay attention to the DPLL (Digital Phase Lock Loop) capability of the MPC850 SCC2 and SCC3 serial ports. The DPLL circuit allows recovering clock information from the serial receive data signal. This

capability, combined with the data encoding options (NRZ, NRZI mark, NRZI space, FM0, FM1, manchester and differential manchester) and protocol options supported by the MPC850, create surprising flexibility in networking support by the MPC8xx processors family.

Pin	Signal Name	Description
1	VDD	+VDD (3.3 Volts) connection on the PPCMB/850.
2	VDD	+VDD (3.3 Volts) connection on the PPCMB/850.
3	TX_EN	Transmit enable input to the serial port driver (CMOS level, positive logic), pulled down.
4	!RX_EN	Receive enable input to the serial port driver (CMOS level, negative logic), pulled down.
5	RTS	Request To Send signal (CMOS level, positive logic) output from the PPCMB/850.
6	RTS	Request To Send signal (CMOS level, positive logic) output from the PPCMB/850.
7	RX+	Differential RS422/RS485 receiver signal A. If A > B by 200mV, the RXD3/SMRXD1 input to the processor will be high (“mark” condition); if A < B by 200mV, the RXD3/SMRXD1 input will be low (“space” condition).
8	RX-	Differential RS422/RS485 receiver signal B.
9	TX-	Differential RS422/RS485 transmitter output signal Z.
10	TX+	Differential RS422/RS485 transmitter output signal Y. A high on TXD3/SMTXD1 (“mark” condition) forces output Y high and output Z low. Similarly, a low on TXD3/SMTXD1 (“space” condition) forces output Y low and output Z high.

Table 3. PPCMB/850 Connector J3 Pinout

Note that for simple UART protocols such as a system console, the MPC850 SMC1 internal peripheral (instead of the MPC850 SCC3 internal peripheral) can be routed to the RS422/RS485 port. This allows a PPCMB/850 application to use the two SCCs for more demanding application-specific networking requirements.

6.3 RS422/RS485 Serial Port Configuration

The PPCMB/850 RS422/RS485 serial port configuration is achieved with jumpers in the positions pairs 1-3, 3-5, 2-4, and 4-6 on the J3 connector, and sometimes with the RTS3 output or the PC13 parallel output pin, as shown in table 4 on page 19.

RS422/RS485 Receiver Configuration		
Jumper configuration on J3 contact pairs 2-4 and 4-6	Jumper on contacts 2-4	Receiver is disabled
	No jumper	Receiver is enabled
	Jumper on contacts 4-6	Receiver is enabled only when the MPC850 de-asserts !RTS3 (i.e. sets PC13 to one)
RS422/RS485 Transmitter Configuration		
Jumper configuration on J3 contact pairs 1-3 and 3-5	Jumper on contacts 1-3	Transmitter is enabled
	No jumper	Transmitter is disabled
	Jumper on contacts 3-5	Transmitter is enabled only when the MPC850 asserts !RTS3 (i.e. sets PC13 to zero)

Table 4. RS422/RS485 Serial Port Hardware Configuration

7. Memory Subsystem

The MPC850 chip select signals CS0 and CS4 are reserved for the PPCMB/850 memory subsystem, respectively for the flash memory and the SRAM memory. In both cases, the MPC850 memory controller GPCM functional block (General Purpose Chip-select Machine) should be used to control the respective memory accesses (BR0(MS)=0, BR4(MS)=0), the port size is 32 bits (BR0(PS)=0, BR4(PS)=0), internal transfer acknowledge is used (OR4(SETA)=0, OR4(SETA)=0), and memory parity checking is not implemented (BR0(PARE)=0, BR4(PARE)=0).

The other chip select signals are available to the host application PCB for memory-based system expansion.

7.1 Flash Memory

The PPCMB/850 flash memory is made of two 16-bits wide flash integrated circuits. The manufacturer is AMD, and the actual part is one of the Am29LV160D parts (the datasheet is reference 6). This gives a total flash memory size of 4MB and a normal flash sector size of 128KB with efficient 32-bits accesses by the MPC850.

If the user relies on CONNOTECH-provided software for the flash memory interface, he is not directly concerned with the details of the flash memory integrated circuit. Otherwise, the user-developed software should read the flash device ID to identify the actual flash memory component among the CONNOTECH issued manufacturing option list, and interface to the flash

integrated circuit accordingly.

No use is made of the hardware protection feature of the flash integrated circuits.

[[Qualified data needed for memory controller registers OR0 and BR0 configuration, based on external clock frequency and the SCCR(EBDF) field. Relevant fields: OR0(CSNT), OR0(ACS), OR0(SCY), OR0(TRLX), OR0(EHTR).]]

7.2 SRAM Memory

The PPCMB/850 flash memory is made of two 16-bits wide flash integrated circuits, each providing a memory capacity of 512KB. This gives a total SRAM memory size of 1MB with efficient 32-bits accesses by the MPC850.

[[Qualified data needed for memory controller registers OR4 and BR4 configuration, based on external clock frequency and the SCCR(EBDF) field. Relevant fields: OR4(CSNT), OR4(ACS), OR4(SCY), OR4(TRLX), OR4(EHTR).]]

For the MPC823 or MPC823E processor variants, the video/LCD controller operation requires the use of burst memory accesses, which is possible only if the MPC850 memory controller UPM functional block (User Programmable Machine) is used instead of the GPCM. Before relying on the MPC823 video/LCD capability, a system hardware designer should check the SRAM burst cycle UPM configuration support status with CONNOTECH.

8. Host Application Board Interface

The PPCMB/850 connectors J1 and J2 are the host application board interface. The pinout of the these connectors is shown in tables 8 (page 25) and 9 (page 26). The J1 and J2 connector arrangement is 4 rows by 26 positions. If the system application electronics does not use the memory bus, only 2 rows of J1 and 2 rows of J2 are actually used (J1 rows C and D and J2 rows A and B).

Every signals on the on the host application board interface have 33 Ohms damping resistors.

8.1 Memory Bus

The memory bus signal groups are shown in table 5 on page 21. The table indicates which bus signals are tied to a 4.7 K-Ohm resistor on the PPCMB/850.

Signal Category	Signal Count	Signal Names
Bus Data Lines	32	D0 to D31
Buss Address Lines	26	A0 to A25
Essential PowerPC Bus Control Lines	6	RD/!WR, !TS (pull-up), TSIZ[0..1], !TA (pull-up), !TEA (pull-up)
Essential MPC8xx Memory Controller Signals	5	!OE, !WE[0..3]
PPCMB/850 Memory Control Lines	4	!WB[0..3]
Burst Cycle Support Signals	3	!BDIP/!GPL_B5, !BI (pull-up), !BURST
Bus Reservation Signals	3	!BR (pull-up), !BG, !BB (pull-up)
Other Signals Controlled by the MPC850 Memory Controller	12	!CS[1..3], !CS[5..7], !CS2/!GPL_A2/!GPL_B2, !CS3/!GPL_A3/!GPL_B3, !GPL_A0/!GPL_B0, !GPL_B4/UPMWAITB, !GPL_A4/UPMWAITA/!AS, !GPL_A5

Table 5. PPCMB/850 Memory Bus Expansion Signal Groups

In implementing external memory devices that terminate the bus cycles with the !TA signal (external transfer acknowledge), it is sometimes observed that a 4.7 K-Ohm pull-up resistor does not provide a fast enough !TA signal rise time. For this reason, the !TA signal is pulled-up on the PPCMB/850 by two 4.7 K-Ohm resistors in parallel, one of them being the discrete resistor R10. In testing new hardware designs, it is possible to experiment with other values for the resistor R10. The figure 5 on page 10 shows the resistors locations on the PPCMB/850 PCB. The resistor R10 is a “0805” resistor component.

DOCUMENTATION WARNINGS

The PPCMB/850 hardware documentation refers to data and address lines using the power-of-two bit weight notation. For instance, the least significant bit of a 32 bits memory access is the data line labeled D0 and the address lines that selects an even or odd numbered byte in an 8-bit access is labeled A0. This notation is prevailing in the datasheets of integrated circuits that are connected to micrprocessor busses. *The Motorola PowerPC documentation uses a reversed notation* (e.g. the PPCMB/850 highest address line A25 is the MPC850 address line A6), presumably inherited from the mainframe culture of the IBM partner at the outset of the PowerPC architecture definition.

No attention is paid to the possible use of the MPC850 device in little-endian mode.

No attention is paid to the Address Type signals documentation, since it is deemed of little use. The AT1 signal from the MPC850 is left unconnected.

The data parity signals DP[0..3] and the multi-processor reservation protocol signals !RSV and !KR/!RETRY are documented with their alternate usage as !IRQx signals.

Note that the MPC850 external DMA capability is neither part of the memory bus subsystem nor part of the memory controller. It is among the integrated peripherals, part of the CP module (see annex A on page 28).

The PPCMB/850 facilitates the memory bus interfacing for SRAM-like memory devices with the signals !WB[0..3]. The truth table for these output signals is the table 6 on page 23.

Inputs			Output
!WR	!WEx	!OE	!WBx
Low	Low	Low	Low
Low	Low	High	Low
Low	High	Low	Low
Low	High	High	High
High	Low	Low	Low
High	Low	High	High
High	High	Low	Low
High	High	High	High

Table 6. Truth Table for PPCMB/850 Memory Bus Signals !WB[0..3]

8.2 Peripherals and Parallel I/O

The PPCMB/850 parallel I/O signals comprise the external signals from three MPC850 functional blocks: the CP (Communications Processor), the PCMCIA interface logic block, and the SIU (System Integration Unit). See table 7 on page 24.

Three of the CP external signals are used locally on the PPCMB/850 for the RS422/RS485 serial port and are also available on the host application board interface connectors. The serial port hardware can be configured so that the host application controls these signals.

Since the PCMCIA interface is essentially not supported by the PCMB/850 design, the PCMCIA input signals are documented as general purpose inputs. Also, the PCMCIA output signals are dedicated to the diagnostic LED control function and the PCMCIA-specific !WAIT_B signal is locally tied to a pull-up resistor, and not available externally.

For ordinary interrupt request inputs, it is recommended to use the !IRQ1 to !IRQ7 signals in preference to the !IRQ0 signal since the latter is not maskable and more challenging for control software if the system state has to be preserved after the interrupt signal servicing. The !IRQ0 use is appropriate only when the desired system reaction to an interrupt signal is analogue to an external reset event.

More generally, the annex B of this document summarizes the external interrupt capability of the MPC850.

Signal Category	Signal Count	Signal Names
Communications Processor	49	PA[4..9], PA[12..15], PB[16..19], PB[22..31], PC[4..15], PD[3..15], See table 11 in annex A on page 28 for internal peripherals functions assigned to these signals.
PCMCIA General Purpose Inputs	8	IP_B[0..7]
SIU (System Interface Unit) Interrupt Signals	9	IRQ[0..7] (two external !IRQ4 are OR'ed in the MPC850)

Table 7. PPCMB/850 Parallel I/O Signal Groups

8.3 Miscellaneous Signals

The two reset signals !PORESET and !HRESET are discussed in section 5.1.3 (page 10) of this document.

The CLKOUT signal is an output clock signal from the MPC850 with the same frequency as the memory bus. It is not used by the PPCMB/850 itself but it is available for system application electronics.

The TEXP signal is a timer expiry signal closely related to power management function. It is not used by the PPCMB/850 itself but it is available for system application electronics. The most likely usage for this signal is to switch power-hungry electronics to low power modes

The host application board connectors has 41 contacts for ground, 4 contacts for +VDD (+3.3 Volts) and 2 reserved contacts (not connected).

	J1, row A	J1, row B	J1, row C	J1, row D
1	D16: !WE0/!BS_AB0	E16: !WE1/!BS_AB1	GND	+VDD
2	M1: D31	L1: D30	GND	N4: PD[3]
3	J2: D29	J1: D28	GND	P3: PD[4]
4	L2: D27	H1: D26	GND	P2: PD[5]
5	F1: D25	E1: D24	GND	R1: PD[6]
6	M2: D23	K2: D22	GND	R2: PD[7]
7	K3: D21	K1: D20	GND	T1: PD[8]
8	M4: D19	M3: D18	GND	P4: PD[9]
9	J3: D17	J4: D16	GND	T2: PD[10]
10	!WB0	!WB1	GND	N5: PD[11]
11	reserved	reserved	GND	R3: PD[12]
12	C13: RD/!WR	D10: !TS	GND	P5: PD[13]
13	A12: !TA	D1: CLKOUT	GND	T3: PD[14]
14	D13: !CS5	B15: !CS7	GND	R4: PD[15]
15	L13: A21	M16: A20	GND	N7: L1ST3 PB[17]
16	M14: A19	L14: A18	GND	R7: L1ST1 PB[19]
17	L15: A17	L16: A16	GND	N14: !SPISEL PB[31]
18	K14: A15	K13: A14	T15: BRGO3 SPIMISO PB[28]	P14: RXD3 SPIMOSI PB[29]
19	G13: A13	K15: A12	T6: CLK3/TIN2/L1TCLKA BRGO2 PA[5]	P15: TXD3 SPICLK PB[30]
20	J15: A11	J14: A10	GND	P6: !CTS3 !SDACK1 L1TSYNCA PC[5]
21	G14: A9	H15: A8	T4: !CD3 L1RSYNCA PC[4]	P13: !RTS3 L1ST7 PC[13]
22	H13: A7	H14: A6	T11: RXD3 SMRXD1 PB[24]	N11: TXD3 SMTXD1 PB[25]
23	F14: A5	K16: A4	GND	T10: !SMSYN1 !SDACK1 PB[23]
24	G16: A3	H16: A2	C2: !IRQ6 DP3	R16: L1ST5 !DREQ0 PC[15]
25	G15: A1	F16: A0	P12: BRGO2 I2CSCL PB[26]	T14: BRGO1 I2CSDA PB[27]
26	F15: TSIZ0	E15: TSIZ1	GND	+VDD

Table 8. PPCMB/850 Connector J1 Pinout

	J2, row A	J2, row B	J2, row C	J2, row D
1	+VDD	GND	D15: !WE2/!BS_AB2	F13: !WE3/!BS_AB3
2	R13: TXD2 PA[12]	R14: RXD2 PA[13]	GND	H2: D15
3	P7: !RTS2 L1ST2 PB[18]	R8: !CTS2 PC[9]	K4: D14	H3: D13
4	N8: !CD2 !TGATE1 PC[8]	T16: L1ST6 !RTS2 !DREQ1 PC[14]	GND	G2: D12
5	R9: !SMSYN2 !SDACK2 PB[22]	GND	G3: D11	F2: D10
6	T9: SMTXD2 L1RXDA PA[8]	N10: SMRXD2 L1TXDA PA[9]	GND	H4: D9
7	T8: CLK1/TIN1/L1RCLKA BRGO1 PA[7]	P8: CLK2/TIN3 !TOUT1 PA[6]	L4: D8	F3: D7
8	P9: USBRXN !TGATE1 PC[10]	N6: USBTXN PC[6]	GND	G4: D6
9	P16: USBRXD PA[15]	GND	E4: D5	L3: D4
10	R10: USBRXP PC[11]	T5: USBTXP PC[7]	GND	F4: D3
11	R15: !USBOE PA[14]	GND	E2: D2	D2: D1
12	R5: L1ST4 !L1RQA PB[16]	T13: L1ST8 !L1RQA PC[12]	GND	E3: D0
13	R6: CLK4/TIN4 !TOUT2 PA[4]	A8: IP_B0	!WB2	!WB3
14	C8: IP_B1	D7: IP_B2	GND	M13: A25
15	A9: IP_B3	GND	N15: A24	N16: A23
16	B9: IP_B4	C9: IP_B5	GND	M15: A22
17	C7: IP_B6	D8: IP_B7	A14: !CS1	C14: !CS6
18	D3: !IRQ5 DP2	N3: !IRQ7	GND	E13: !GPL_A0/!GPL_B0
19	D4: !IRQ4 DP1	GND	C16: !GPL_A1/!GPL_B1/!OE	B13: !GPL_B4/UPMWAITB
20	D9: !IRQ2 !RSV	C3: !IRQ3 DP0	GND	D11: !GPL_A4/UPMWAITA !AS
21	N1: !IRQ0	N2: !IRQ1	A13: !BDIP !GPL_B5	C12: !GPL_A5
22	B3: !PORESET	D5: TEXP	GND	C11: !TEA
23	B5: !HRESET	GND	B11: !BR	C10: !BG
24	B14: !CS2	A15: !CS3	GND	A11: !BB
25	C15: !CS2 !GPL_A2/!GPL_B2	D14: !CS3 !GPL_A3/!GPL_B3	B12: !BI	B10: !BURST
26	+VDD	GND	B7: !IRQ4 !KR/!RETRY	GND

Table 9. PPCMB/850 Connector J2 Pinout

9. PPCMB/850 Manufacturing Options

The PPCMB/850 manufacturing options listed in table 10 on page 27.

Manufacturing Option	Typical Setting	Design Options
MPC8xx Part	100-0001-01, Motorola XPC850DEZT50BT	Every flavor of the Motorola MPC850, MPC823, and MPC823e processors
Flash Memory Part	104-0001-01, AMD Am29LV160DT-90EI	AMD Am29LV160... (4MB total), Am29LV800... (2MB total), Am29LV400... (1MB total), or compatible devices
Oscillator Frequency	10 MHz	3.6864 MHz, 4 MHz, 6.176 MHz, 7.3728 MHz, 8 MHz, and 10 MHz.
J1 Connector	600-0005-02, 4x26 positions socket connector on the bottom side of the PCB, SAMTEC SQT-126-01-F-Q (the datasheet is reference [8])	4x26 positions through-hole connectors on a 2 mm grid, 2x26 positions connector on the C and D contact rows, through-hole connectors on a 2 mm grid
J2 Connector	Same as J1 connector	4x26 positions through-hole connectors on a 2 mm grid, 2x26 positions connector on the A and B contact rows, through-hole connectors on a 2 mm grid
J3 Connector	.100 inches header on the top side of PCB, 2x5 positions	idem, or not installed
J4 Connector	.100 inches header on the top side of PCB, 2x6 positions	idem, 2x5 positions header, or not installed
Resistor R10	4.7 K-Ohm	4.7K, lower values to be determined, not installed
Resistor R11	not installed	0 Ohm, not instaled
Resistor R12	not installed	0 Ohm, not installed
Industrial Temperature Option	No	Yes, No

Table 10. PPCMB/850 Manufacturing Options

Annex A - MPC850 Integrated Peripherals Signal Multiplexing

Paral-lel I/O	USB	SMC1	SMC2	SCC2	SCC3	IDMA	SPI	I2C	Serial Interface	Clocks
PA[4]										CLK4/TIN4 !TOUT2
PA[5]									L1TCLKA	CLK3/TIN2 BRGO2
PA[6]										CLK2/TIN3 !TOUT1
PA[7]									L1RCLKA	CLK1/TIN1 BRGO1
PA[8]			SMTXD2						L1RXDA	
PA[9]			SMRXD2						L1TXDA	
PA[12]				TXD2						
PA[13]				RXD2						
PA[14]	!USBOE									
PA[15]	USBRXD									
PB[16]									L1ST4 !L1RQA	
PB[17]									L1ST3	
PB[18]				!RTS2					L1ST2	
PB[19]									L1ST1	
PB[22]			!SMSYN2			!SDACK2				
PB[23]		!SMSYN1				!SDACK1				
PB[24]		SMRXD1			RXD3					
PB[25]		SMTXD1			TXD3					
PB[26]								I2CSCL		BRGO2

Paral-lel I/O	USB	SMC1	SMC2	SCC2	SCC3	IDMA	SPI	I2C	Serial Interface	Clocks
PB[27]								I2CSDA		BRGO1
PB[28]							SPIMISO			BRGO3
PB[29]					RXD3		SPIMOSI			
PB[30]					TXD3		SPICLK			
PB[31]							!SPISEL			
PC[4]					!CD3				L1RSYNCA	
PC[5]					!CTS3	!SDACK1			L1TSYNCA	
PC[6]	USBTXN									
PC[7]	USBTXP									
PC[8]				!CD2						!TGATE1
PC[9]				!CTS2						
PC[10]	USBRXN									!TGATE1
PC[11]	USBRXP									
PC[12]									L1ST8 !L1RQA	
PC[13]					!RTS3				L1ST7	
PC[14]				!RTS2		!DREQ1			L1ST6	
PC[15]						!DREQ0			L1ST5	

Table 11. MPC850 Integrated Peripherals Signal Multiplexing

Annex B - External Interrupt Sources

The material in this annex should assist the system hardware designer in assigning external signals that can use the MPC850 interrupt responsiveness capability.

The MPC850 features a number of external signals that may trigger an interrupt to the core. Since their documentation is spread in various sections of the MPC850 User Manual, it is not always obvious to use the MPC850 hardware capabilities for handling external discrete inputs. Here is a summary list of external interrupt sources for the MPC850, with indications of relevant interrupt capabilities. The interrupt capabilities are indicated for falling edge detection (‾_), low level detection (_), detection of any change in the logic level (_/‾_), high level detection (‾), and raising edge detection (_/‾).

The list below also includes indications of alternate uses of each signal (where applicable) in broad terms. Neither the MPC850 TDMA serial interface nor the MPC850 features reserved and/or omitted in the PPCMB/850 design are taken into account in preparing this list. The exact specifications from the MPC850 documentation should be used to verify the final system design.

Input Signal	PPCMB/850 connector, pin	Description / alternate use of the signal	Edge and level interrupt capability				
			‾_	__	_/‾_	‾‾	_/‾
IRQ0	J2, A21	Special purpose IRQ0 input signal, a non-maskable interrupt source	‾_	__			
IRQ1	J2, B21	General purpose IRQ1 input signal	‾_	__			
IRQ2	J2, A20	General purpose IRQ2 input signal / Memory reservation protocol, !RSV	‾_	__			
IRQ3	J2, B20	General purpose IRQ3 input signal / Memory data parity DP0	‾_	__			
IRQ4	J2, A19 and J2, C26	General purpose IRQ4 input signal / Memory data parity DP1 (on J2, A19) // Memory reservation protocol, !KR (on J2, C26)	‾_	__			
IRQ5	J2, A18	General purpose IRQ5 input signal / Memory data parity DP2	‾_	__			

Input Signal	PPCMB/850 connector, pin	Description / alternate use of the signal	Edge and level interrupt capability				
			¯_	__	¯X¯	¯¯	_/¯
IRQ6	J1, C24	General purpose IRQ6 input signal / Memory data parity DP3	¯_	__			
IRQ7	J2, B18	General purpose IRQ7 input signal	¯_	__			
PC4	J1, C21	Parallel I-O PC4 / SCC3, !CD3 input	¯_		¯X¯		
PC5	J1, D20	Parallel I-O PC5 / SCC3, !CTS3 input / IDMA channel 1 acknowledge output	¯_		¯X¯		
PC6	J2, B8	Parallel I-O PC6 / USB, USBTXN output	¯_		¯X¯		
PC7	J2, B10	Parallel I-O PC7 / USB, USBTXP	¯_		¯X¯		
PC8	J2, A4	Parallel I-O PC8 / SCC2, !CD2 input / CP Timer 1&2 gate input	¯_		¯X¯		
PC9	J2, B3	Parallel I-O PC9 / SCC2, !CTS2 input	¯_		¯X¯		
PC10	J2, A8	Parallel I-O PC10 / USB, USBRXN	¯_		¯X¯		
PC11	J2, A10	Parallel I-O PC11 / USB, USBRXP	¯_		¯X¯		
PC12	J2, B12	Parallel I-O PC12	¯_		¯X¯		
PC13	J1, D21	Parallel I-O PC13 / SCC3, !RTS3 output	¯_		¯X¯		
PC14	J2, B4	Parallel I-O PC14 / SCC2, !RTS2 output / IDMA channel 2 request input	¯_		¯X¯		
PC15	J1, D24	Parallel I-O PC15 / IDMA channel 1 request input	¯_		¯X¯		

Input Signal	PPCMB/850 connector, pin	Description / alternate use of the signal	Edge and level interrupt capability				
			¯_	__	¯X¯	¯¯	_/¯
IP_B0	J2, B13	“CBVS1” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B1	J2, A14	“CBVS2” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B2	J2, B14	“CBWP” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B3	J2, A15	“CBCD2” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B4	J2, A16	“CBCD1” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B5	J2, B16	“CBBVD2” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B6	J2, A17	“CBBVD1” in the MPC850 PCMCIA interface documentation			¯X¯		
IP_B7	J2, B17	“CBRDY” in the MPC850 PCMCIA interface docmentation	¯_	__	¯X¯	¯¯	_/¯

Annex C - Index of Signal Names

.1 Signals Available in the J1 and J2 Connectors

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
A0	A0	J1/B25	F16
A1	A1	J1/A25	G15
A2	A2	J1/B24	H16
A3	A3	J1/A24	G16
A4	A4	J1/B23	K16
A5	A5	J1/A23	F14
A6	A6	J1/B22	H14
A7	A7	J1/A22	H13
A8	A8	J1/B21	H15
A9	A9	J1/A21	G14
A10	A10	J1/B20	J14
A11	A11	J1/A20	J15
A12	A12	J1/B19	K15
A13	A13	J1/A19	G13
A14	A14	J1/B18	K13
A15	A15	J1/A18	K14
A16	A16	J1/B17	L16
A17	A17	J1/A17	L15
A18	A18	J1/B16	L14
A19	A19	J1/A16	M14
A20	A20	J1/B15	M16
A21	A21	J1/A15	L13
A22	A22	J2/D16	M15
A23	A23	J2/D15	N16
A24	A24	J2/C15	N15

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
A25	A25	J2/D14	M13
!AS	!GPL_A4/UPMWAITA !AS	J2/D20	D11
!BB	!BB	J2/D24	A11
!BDIP	!BDIP !GPL_B5	J2/C21	A13
!BG	!BG	J2/D23	C10
!BI	!BI	J2/C25	B12
!BR	!BR	J2/C23	B11
BRGO1	CLK1/TIN1/L1RCLKA BRGO1 PA[7]	J2/A7	T8
BRGO1	BRGO1 I2CSDA PB[27]	J1/D25	T14
BRGO2	BRGO2 I2CSCL PB[26]	J1/C25	P12
BRGO2	CLK3/TIN2/L1TCLKA BRGO2 PA[5]	J1/C19	T6
BRGO3	BRGO3 SPIMISO PB[28]	J1/C18	T15
!BS_AB0	!WE0/!BS_AB0	J1/A1	D16
!BS_AB1	!WE1/!BS_AB1	J1/B1	E16
!BS_AB2	!WE2/!BS_AB2	J2/C1	D15
!BS_AB3	!WE3/!BS_AB3	J2/D1	F13
!BURST	!BURST	J2/D25	B10
!CD2	!CD2 !TGATE1 PC[8]	J2/A4	N8
!CD3	!CD3 L1RSYNCA PC[4]	J1/C21	T4
CLK1	CLK1/TIN1/L1RCLKA BRGO1 PA[7]	J2/A7	T8
CLK2	CLK2/TIN3 !TOUT1 PA[6]	J2/B7	P8
CLK3	CLK3/TIN2/L1TCLKA BRGO2 PA[5]	J1/C19	T6
CLK4	CLK4/TIN4 !TOUT2 PA[4]	J2/A13	R6
CLKOUT	CLKOUT	J1/B13	D1
!CS1	!CS1	J2/C17	A14
!CS2	!CS2	J2/A24	B14
!CS2	!CS2 !GPL_A2/!GPL_B2	J2/A25	C15
!CS3	!CS3 !GPL_A3/!GPL_B3	J2/B25	D14

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
!CS3	!CS3	J2/B24	A15
!CS5	!CS5	J1/A14	D13
!CS6	!CS6	J2/D17	C14
!CS7	!CS7	J1/B14	B15
!CTS2	!CTS2 PC[9]	J2/B3	R8
!CTS3	!CTS3 !SDACK1 L1TSYNCA PC[5]	J1/D20	P6
D0	D0	J2/D12	E3
D1	D1	J2/D11	D2
D2	D2	J2/C11	E2
D3	D3	J2/D10	F4
D4	D4	J2/D9	L3
D5	D5	J2/C9	E4
D6	D6	J2/D8	G4
D7	D7	J2/D7	F3
D8	D8	J2/C7	L4
D9	D9	J2/D6	H4
D10	D10	J2/D5	F2
D11	D11	J2/C5	G3
D12	D12	J2/D4	G2
D13	D13	J2/D3	H3
D14	D14	J2/C3	K4
D15	D15	J2/D2	H2
D16	D16	J1/B9	J4
D17	D17	J1/A9	J3
D18	D18	J1/B8	M3
D19	D19	J1/A8	M4
D20	D20	J1/B7	K1
D21	D21	J1/A7	K3

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
D22	D22	J1/B6	K2
D23	D23	J1/A6	M2
D24	D24	J1/B5	E1
D25	D25	J1/A5	F1
D26	D26	J1/B4	H1
D27	D27	J1/A4	L2
D28	D28	J1/B3	J1
D29	D29	J1/A3	J2
D30	D30	J1/B2	L1
D31	D31	J1/A2	M1
DP0	!IRQ3 DP0	J2, B20	C3
DP1	!IRQ4 DP1	J2, A19	D4
DP2	!IRQ5 DP2	J2, A18	D3
DP3	!IRQ6 DP3	J1, C24	C2
!DREQ0	L1ST5 !DREQ0 PC[15]	J1/D24	R16
!DREQ1	L1ST6 !RTS2 !DREQ1 PC[14]	J2/B4	T16
GND	GND	J1/C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C20, C23, C26, J2/B1, B5, B9, B11, B15, B19, B23, B26, C2, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, D26	
!GPL_A0	!GPL_A0/!GPL_B0	J2/D18	E13
!GPL_A1	!GPL_A1/!GPL_B1/!OE	J2/C19	C16
!GPL_A2	!CS2 !GPL_A2/!GPL_B2	J2/A25	C15
!GPL_A3	!CS3 !GPL_A3/!GPL_B3	J2/B25	D14
!GPL_A4	!GPL_A4/UPMWAITA !AS	J2/D20	D11
!GPL_A5	!GPL_A5	J2/D21	C12
!GPL_B0	!GPL_A0/!GPL_B0	J2/D18	E13
!GPL_B1	!GPL_A1/!GPL_B1/!OE	J2/C19	C16

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
!GPL_B2	!CS2 !GPL_A2/!GPL_B2	J2/A25	C15
!GPL_B3	!CS3 !GPL_A3/!GPL_B3	J2/B25	D14
!GPL_B4	!GPL_B4/UPMWAITB	J2/D19	B13
!GPL_B5	!BDIP !GPL_B5	J2/C21	A13
!HRESET	!HRESET	J2/A23	B5
I2CSCL	BRGO2 I2CSCL PB[26]	J1/C25	P12
I2CSDA	BRGO1 I2CSDA PB[27]	J1/D25	T14
IP_B0	IP_B0	J2/B13	A8
IP_B1	IP_B1	J2/A14	C8
IP_B2	IP_B2	J2/B14	D7
IP_B3	IP_B3	J2/A15	A9
IP_B4	IP_B4	J2/A16	B9
IP_B5	IP_B5	J2/B16	C9
IP_B6	IP_B6	J2/A17	C7
IP_B7	IP_B7	J2/B17	D8
!IRQ0	!IRQ0	J2, A21	N1
!IRQ1	!IRQ1	J2, B21	N2
!IRQ2	!IRQ2 !RSV	J2, A20	D9
!IRQ3	!IRQ3 DP0	J2, B20	C3
!IRQ4	!IRQ4 DP1	J2, A19	D4
!IRQ4	!IRQ4 !KR/!RETRY	J2, C26	B7
!IRQ5	!IRQ5 DP2	J2, A18	D3
!IRQ6	!IRQ6 DP3	J1, C24	C2
!IRQ7	!IRQ7	J2, B18	N3
!KR	!IRQ4 !KR/!RETRY	J2/C26	B7
L1RCLKA	CLK1/TIN1/L1RCLKA BRGO1 PA[7]	J2/A7	T8
!L1RQA	L1ST4 !L1RQA PB[16]	J2/A12	R5
!L1RQA	L1ST8 !L1RQA PC[12]	J2/B12	T13

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
L1RSYNCA	!CD3 L1RSYNCA PC[4]	J1/C21	T4
L1RXDA	SMTXD2 L1RXDA PA[8]	J2/A6	T9
L1ST1	L1ST1 PB[19]	J1/D16	R7
L1ST2	!RTS2 L1ST2 PB[18]	J2/A3	P7
L1ST3	L1ST3 PB[17]	J1/D15	N7
L1ST4	L1ST4 !L1RQA PB[16]	J2/A12	R5
L1ST5	L1ST5 !DREQ0 PC[15]	J1/D24	R16
L1ST6	L1ST6 !RTS2 !DREQ1 PC[14]	J2/B4	T16
L1ST7	!RTS3 L1ST7 PC[13]	J1/D21	P13
L1ST8	L1ST8 !L1RQA PC[12]	J2/B12	T13
L1TCLKA	CLK3/TIN2/L1TCLKA BRGO2 PA[5]	J1/C19	T6
L1TSYNCA	!CTS3 !SDACK1 L1TSYNCA PC[5]	J1/D20	P6
L1TXDA	SMRXD2 L1TXDA PA[9]	J2/B6	N10
!OE	!GPL_A1/!GPL_B1/!OE	J2/C19	C16
PA[4]	CLK4/TIN4 !TOUT2 PA[4]	J2/A13	R6
PA[5]	CLK3/TIN2/L1TCLKA BRGO2 PA[5]	J1/C19	T6
PA[6]	CLK2/TIN3 !TOUT1 PA[6]	J2/B7	P8
PA[7]	CLK1/TIN1/L1RCLKA BRGO1 PA[7]	J2/A7	T8
PA[8]	SMTXD2 L1RXDA PA[8]	J2/A6	T9
PA[9]	SMRXD2 L1TXDA PA[9]	J2/B6	N10
PA[12]	TXD2 PA[12]	J2/A2	R13
PA[13]	RXD2 PA[13]	J2/B2	R14
PA[14]	!USBOE PA[14]	J2/A11	R15
PA[15]	USBRXD PA[15]	J2/A9	P16
PB[16]	L1ST4 !L1RQA PB[16]	J2/A12	R5
PB[17]	L1ST3 PB[17]	J1/D15	N7
PB[18]	!RTS2 L1ST2 PB[18]	J2/A3	P7
PB[19]	L1ST1 PB[19]	J1/D16	R7

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
PB[22]	!SMSYN2 !SDACK2 PB[22]	J2/A5	R9
PB[23]	!SMSYN1 !SDACK1 PB[23]	J1/D23	T10
PB[24]	RXD3 SMRXD1 PB[24]	J1/C22	T11
PB[25]	TXD3 SMTXD1 PB[25]	J1/D22	N11
PB[26]	BRGO2 I2CSCL PB[26]	J1/C25	P12
PB[27]	BRGO1 I2CSDA PB[27]	J1/D25	T14
PB[28]	BRGO3 SPIMISO PB[28]	J1/C18	T15
PB[29]	RXD3 SPIMOSI PB[29]	J1/D18	P14
PB[30]	TXD3 SPICLK PB[30]	J1/D19	P15
PB[31]	!SPISEL PB[31]	J1/D17	N14
PC[4]	!CD3 L1RSYNCA PC[4]	J1/C21	T4
PC[5]	!CTS3 !SDACK1 L1TSYNCA PC[5]	J1/D20	P6
PC[6]	USBTXN PC[6]	J2/B8	N6
PC[7]	USBTXP PC[7]	J2/B10	T5
PC[8]	!CD2 !TGATE1 PC[8]	J2/A4	N8
PC[9]	!CTS2 PC[9]	J2/B3	R8
PC[10]	USBRXN !TGATE1 PC[10]	J2/A8	P9
PC[11]	USBRXP PC[11]	J2/A10	R10
PC[12]	L1ST8 !L1RQA PC[12]	J2/B12	T13
PC[13]	!RTS3 L1ST7 PC[13]	J1/D21	P13
PC[14]	L1ST6 !RTS2 !DREQ1 PC[14]	J2/B4	T16
PC[15]	L1ST5 !DREQ0 PC[15]	J1/D24	R16
PD[3]	PD[3]	J1/D2	N4
PD[4]	PD[4]	J1/D3	P3
PD[5]	PD[5]	J1/D4	P2
PD[6]	PD[6]	J1/D5	R1
PD[7]	PD[7]	J1/D6	R2
PD[8]	PD[8]	J1/D7	T1

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
PD[9]	PD[9]	J1/D8	P4
PD[10]	PD[10]	J1/D9	T2
PD[11]	PD[11]	J1/D10	N5
PD[12]	PD[12]	J1/D11	R3
PD[13]	PD[13]	J1/D12	P5
PD[14]	PD[14]	J1/D13	T3
PD[15]	PD[15]	J1/D14	R4
!PORESET	!PORESET	J2/A22	B3
RD	RD/!WR	J1/A12	C13
RESERVED	RESERVED	J1/A11, B11	
!RETRY	!IRQ4 !KR/!RETRY	J2/C26	B7
!RSV	!IRQ2 !RSV	J2/A20	D9
!RTS2	L1ST6 !RTS2 !DREQ1 PC[14]	J2/B4	T16
!RTS2	!RTS2 L1ST2 PB[18]	J2/A3	P7
!RTS3	!RTS3 L1ST7 PC[13]	J1/D21	P13
RXD2	RXD2 PA[13]	J2/B2	R14
RXD3	RXD3 SPIMOSI PB[29]	J1/D18	P14
RXD3	RXD3 SMRXD1 PB[24]	J1/C22	T11
!SDACK1	!CTS3 !SDACK1 L1TSYNCA PC[5]	J1/D20	P6
!SDACK1	!SMSYN1 !SDACK1 PB[23]	J1/D23	T10
!SDACK2	!SMSYN2 !SDACK2 PB[22]	J2/A5	R9
SMRXD1	RXD3 SMRXD1 PB[24]	J1/C22	T11
SMRXD2	SMRXD2 L1TXDA PA[9]	J2/B6	N10
!SMSYN1	!SMSYN1 !SDACK1 PB[23]	J1/D23	T10
!SMSYN2	!SMSYN2 !SDACK2 PB[22]	J2/A5	R9
SMTXD1	TXD3 SMTXD1 PB[25]	J1/D22	N11
SMTXD2	SMTXD2 L1RXDA PA[8]	J2/A6	T9
SPICLK	TXD3 SPICLK PB[30]	J1/D19	P15

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
SPIMISO	BRGO3 SPIMISO PB[28]	J1/C18	T15
SPIMOSI	RXD3 SPIMOSI PB[29]	J1/D18	P14
!SPISEL	!SPISEL PB[31]	J1/D17	N14
!TA	!TA	J1/A13	A12
!TEA	!TEA	J2/D22	C11
TEXP	TEXP	J2/B22	D5
!TGATE1	!CD2 !TGATE1 PC[8]	J2/A4	N8
!TGATE1	USBRXN !TGATE1 PC[10]	J2/A8	P9
TIN1	CLK1/TIN1/L1RCLKA BRGO1 PA[7]	J2/A7	T8
TIN2	CLK3/TIN2/L1TCLKA BRGO2 PA[5]	J1/C19	T6
TIN3	CLK2/TIN3 !TOUT1 PA[6]	J2/B7	P8
TIN4	CLK4/TIN4 !TOUT2 PA[4]	J2/A13	R6
!TOUT1	CLK2/TIN3 !TOUT1 PA[6]	J2/B7	P8
!TOUT2	CLK4/TIN4 !TOUT2 PA[4]	J2/A13	R6
!TS	!TS	J1/B12	D10
TSIZ0	TSIZ0	J1/A26	F15
TSIZ1	TSIZ1	J1/B26	E15
TXD2	TXD2 PA[12]	J2/A2	R13
TXD3	TXD3 SMTXD1 PB[25]	J1/D22	N11
TXD3	TXD3 SPICLK PB[30]	J1/D19	P15
UPMWAITA	!GPL_A4/UPMWAITA !AS	J2/D20	D11
UPMWAITB	!GPL_B4/UPMWAITB	J2/D19	B13
!USBOE	!USBOE PA[14]	J2/A11	R15
USBRXD	USBRXD PA[15]	J2/A9	P16
USBRXN	USBRXN !TGATE1 PC[10]	J2/A8	P9
USBRXP	USBRXP PC[11]	J2/A10	R10
USBTXN	USBTXN PC[6]	J2/B8	N6
USBTXP	USBTXP PC[7]	J2/B10	T5

Signal Name	Signal Group	PPCMB/850 Pin	MPC850 Pin
+VDD	+VDD	J1/D1, D26, J2/A1, A26	
!WB0	!WB0	J1/A10	
!WB1	!WB1	J1/B10	
!WB2	!WB2	J2/C13	
!WB3	!WB3	J2/D13	
!WE0	!WE0/!BS_AB0	J1/A1	D16
!WE1	!WE1/!BS_AB1	J1/B1	E16
!WE2	!WE2/!BS_AB2	J2/C1	D15
!WE3	!WE3/!BS_AB3	J2/D1	F13
!WR	RD/!WR	J1/A12	C13

.2 Other MPC850 Signals

The MPC850 signal names not listed in the previous annex are listed below, with an indication of their documentation and/or usage status. This annex is provided as a documentation assistance only.

Signal Name	Signal Group	MPC850 Pin	Documentation and/or Usage Status
ALE_B	ALE_B/DSCK/AT1	B8	Not connected
AT0		C7	Not documented
AT1	ALE_B/DSCK/AT1	B8	Not connected
AT2		D7	Not documented
AT3		D8	Not documented
!CE1_B		C14	Not documented (PCMCIA feature)
!CE2_B		B15	Not documented (PCMCIA feature)
!CS0		D12	Used on the PCB for flash memory chip select
!CS4		B16	Used on the PCB for SRAM memory chip select
DSCK	ALE_B/DSCK/AT1	B8	Not connected
DSCK	TCK/DSCK	T12	Used on the PCB for the BDM or JTAG connection
DSDI		C7	Not documented (BDM or JTAG feature not used)
DSDI	TDI/DSDI	R11	Used on the PCB for the BDM or JTAG connection
DSDO		B6	Not documented (BDM or JTAG feature not used)
DSDO	TDO/DSDO	N12	Used on the PCB for the BDM or JTAG connection
EXTAL		A4	Not connected
EXTCLK		A6	Used on the PCB for the processor clock
FRZ	FRZ/!IRQ6	A10	Used on the PCB for the BDM or JTAG connection
!IOIS16_B		D7	Not documented (PCMCIA feature)
!IORD		D16	Not documented (PCMCIA feature)
!IOWR		E16	Not documented (PCMCIA feature)

Signal Name	Signal Group	MPC850 Pin	Documentation and/or Usage Status
!IRQ6	FRZ/!IRQ6	A10	Used on the PCB for the BDM or JTAG connection
IWP0		A8	Not documented (BDM or JTAG feature not used)
IWP1		C8	Not documented (BDM or JTAG feature not used)
IWP2		A9	Not documented (BDM or JTAG feature not used)
LWP0		B9	Not documented (BDM or JTAG feature not used)
LWP1		C9	Not documented (BDM or JTAG feature not used)
MODCK1		D6	Pulled-up to +VDD during power-on-reset
MODCK2		B6	Pulled-up to +VDD during power-on-reset
OP2		D6	Used on the PCB to drive the troubleshooting LED D2
OP3		B6	Used on the PCB to drive the troubleshooting LED D1
!PCOE		D15	Not documented (PCMCIA feature)
!PCWE		F13	Not documented (PCMCIA feature)
!PTR		D8	Not documented (BDM or JTAG feature not used)
!REG		F15	Not documented (PCMCIA feature)
SPKROUT		B7	Not documented (PCMCIA feature)
!SRESET		B4	Used on the PCB for the BDM or JTAG connection
!STS		D6	Not documented (BDM or JTAG feature not used)
TCK	TCK/DSCK	T12	Used on the PCB for the BDM or JTAG connection
TDI	TDI/DSDI	R11	Used on the PCB for the BDM or JTAG connection
TDO	TDO/DSDO	N12	Used on the PCB for the BDM or JTAG connection
TMS		R12	Used on the PCB for the BDM or JTAG connection
!TRST		P11	Used on the PCB for the BDM or JTAG connection
VF0		B9	Not documented (BDM or JTAG feature not used)
VF1		C9	Not documented (BDM or JTAG feature not used)
VF2		A9	Not documented (BDM or JTAG feature not used)
VFLS0		A8	Not documented (BDM or JTAG feature not used)
VFLS1		C8	Not documented (BDM or JTAG feature not used)
WAIT_B		C4	Connected to a pull-up resistor
XFC		B2	Used on the PCB for the processor clock
XTAL		B4	Not connected